CLAIMS:

1. A system for servicing packet data transactions and input/output transactions within a processing device using common data paths, the system comprising:

an input port that is operable to receive communications from a communicatively coupled processing device, the communications including packet data transactions and input/output transactions;

an output port that is operable to transmit communications to a communicatively coupled processing device, the communications including packet data transactions and input/output transactions;

a node controller communicatively coupled to a system bus of the processing device that is operable to service input/output transactions;

a packet manager communicatively coupled to the system bus of the processing device that is operable to service packet data transactions; and

a switching module communicatively coupled to the input port, the output port, the node controller, and the packet manager, wherein the switching module is operable to service the exchange of transaction cells among the input port, the output port, the node controller, and the packet manager, each transaction cell having a control tag and data and carrying all or a portion of a packet data transaction or an input/output transaction.

2. The system of claim 1, further comprising an agent status information table used by the switching module to schedule the exchange of transaction cells among the input port, the output port, the node controller, and the packet manager.

3. The system of claim 1, wherein the input port and/or the output port support both a packet based interface and an address based interface.

4. The system of claim 3, wherein:

the packet based interface is a SPI-4 interface; and

the address based interface is one of a HyperTransport interface, a PCI interface, a PCI-X interface, or a PCI Express interface.

5. The system of claim 1, wherein the input/output transactions comprise read transactions, write transactions, cache coherency transactions, and responses.

6. The system of claim 1, wherein the packet data transactions comprise packet data transfers between the processing device and another processing device coupled to the processing device via the input port and/or the output port.

7. The system of claim 1, further comprising

at least one additional input port communicatively coupled to the switching module;

at least one additional output port communicatively coupled to the switching module; and

wherein the switching module communicates with the at least one additional input port and the at least one additional output port using transactions cells.

8. The system of claim 1, wherein the control tag comprises:

a first set of information when the transaction cell corresponds to a packet data transaction; and

a second set of information when the transaction cell corresponds to an input/output transaction.

9. The system of claim 1, wherein when a transaction cell corresponds to a packet data transaction the control tag comprises:

a transaction cell data bit count;

an input virtual channel identifier; and

a packet data source identifier.

10. The system of claim 1, wherein when a transaction cell corresponds an input/output transaction the control tag comprises:

a first set of information when the transaction cell corresponds to non-response input/output transaction; and

a second set of information when the transaction cell corresponds to a response input/output transaction.

11. The system of claim 10, wherein:

the first set of information includes a command bit and a flush bit; and

the second set of information includes a command bit, information concerning forwarding of the input/output transaction, and a flush bit.

12. The system of claim 1, wherein:

a response input/output transaction occupies a single transaction cell;

a control tag of the single transaction cell carries a control portion of the response input/output transaction; and

data of the single transaction cell carries a data portion of the response input/output transaction.

13. The system of claim 1, wherein:

each input/output transaction occupies a plurality of transaction cells;

when the input/output transaction is a response, a control tag of a first transaction cell carries a control portion of the input/output transaction and data of the first transaction cell carries a data portion of the input/output transaction; and

when the input/output transaction is not a response, data of a first transaction cell carries a control portion of the input/output transaction and data of a second transaction cell carries a data portion of the input/output transaction.

14. The system of claim 1, wherein:

a control field of non-response input/output transaction is mapped to a first transaction cell; and

a data field of the non-response input/output transaction is mapped to at least one of 2nd-5th transaction cells.

15. The system of claim 14, wherein:

a control field of response input/output transaction is mapped to a control tag of a first transaction cell; and

a data field of the response input/output transaction is mapped to data of the first transaction cell and to data of at least one of 1st-4th transaction cells.

16. The system of claim 1, wherein:

the packet data transaction occupies a plurality of transaction cells; and

a control tag of each transaction cell of the plurality of transaction cells carries a control portion of the packet data transaction.

17. The system of claim 1, wherein the switching module supports the multicasting of transaction cells between the input port, the output port, the node controller, and the packet manager.

18. A method for servicing packet data transactions and input/output transactions within a processing device using a common data path, the method comprising:

receiving communications from a communicatively coupled processing device at an input port, the communications including packet data transactions and input/output transactions;

transmitting communications to a communicatively coupled processing device from an output port, the communications including packet data transactions and input/output transactions;

servicing input/output transactions using a node controller;

servicing packet data transactions using a packet manager;

forming transaction cells at the input port, the node controller, and the packet managers, each transaction cell having a control tag and data and carrying all or a portion of a packet data transaction or an input/output transaction; and

passing transaction cells between the input port, the output port, the node controller, and the packet managers on the common data path.

19. The method of claim 18, further comprising scheduling the exchange of transaction cells among the input port, the output port, the node controller, and the packet manager based upon the management of control information.

20. The method of claim 18, further comprising supporting both a packet-based interface and an input/output-based interface at the input port and the output port.

21. The method of claim 20, wherein:

the packet-based interface is a SPI-4 interface; and

the input/output-based interface is one of a HyperTransport interface, a PCI interface, a PCI-X interface, or a PCI Express interface.

22. The method of claim 18, wherein the input/output transactions comprise read transactions, write transactions, and cache coherency transactions.

23. The method of claim 18, wherein the packet data transactions comprise packet data transfers between the processing device and another processing device coupled to the processing device via the input port and/or the output port.

24. The method of claim 18, wherein the control tag comprises:

a first set of information when the transaction cell corresponds to a packet data transaction; and

a second set of information when the transaction cell corresponds to an input/output transaction.

25. The method of claim 18, wherein when a transaction cell corresponds to a packet data transaction the control tag comprises:

a transaction cell data bit count;

an input virtual channel identifier; and

a packet data source identifier.

26. The method of claim 18, wherein when a transaction cell corresponds an input/output transaction the control tag comprises:

a first set of information when the transaction cell corresponds to non-response input/output transaction; and

a second set of information when the transaction cell corresponds to a response input/output transaction.

27. The method of claim 26, wherein:

the first set of information includes a command bit and a flush bit; and

the second set of information includes a command bit, information concerning forwarding of the input/output transaction, and a flush bit.

28. The method of claim 18, further comprising forming a transaction cell to carry a non-response input/output transaction by:

placing a control field of the non-response input/output transaction in a data portion of a first transaction cell; and

placing a data field of the non-response input/output transaction in data portions of subsequent transaction cells.

29. The method of claim 18, further comprising forming a transaction cell to carry a response input/output transaction by:

placing a control portion of the response input/output transaction into a control tag of a single transaction cell; and

placing a data field of the response input/output transaction into a data portion of the input/output transaction.

30. The method of claim 18, further comprising forming a transaction cell to carry response input/output transactions by:

placing a control field of the response input/output transaction in a control tag of a first transaction cell; and

placing a data field of the response input/output transaction in data portions of the first transaction cell and subsequent transaction cells.

31. The method of claim 18, further comprising multicasting transaction cells between the input port, the output port, the node controller, and the packet manager.